CLAIMS

1. In a broadband earliest deadline first (EDF) queue integrated circuit, a method for sorting information by field rank, the method comprising:

extracting information segments having a field with a sequential rank, by field rank, at a maximum extraction rate; and

inserting information segments, at a maximum insertion rate equal to twice the maximum extraction rate.

2. The method of claim 1 wherein inserting information segments includes inserting information segments into a temporary register.

3. The method of claim 2 further comprising:

systolically moving information segments with lower field ranks to registers higher in a sequenced order of registers.

4. The method of claim 3 further comprising:

systolically moving information segments with higher field ranks to registers lower in a sequenced order of registers.

5. The method of claim 4 further comprising:

pairing temporary registers with corresponding permanent registers having the same order in a sequence of neighboring registers, forming stages in a sequenced order of stages.

6. In a broadband earliest deadline first (EDF) queue, a method for sorting information segments by field rank, the method comprising:

systolically moving information segments with lower field ranks to temporary registers higher in a sequenced order of temporary registers;

systolically moving information segments with higher field ranks to permanent registers lower in a sequenced order of permanent registers; and

pairing each temporary register with a corresponding permanent register having the same order in a sequence of neighboring registers, forming stages in a sequenced order of stages.

7. The method of claim 6 further comprising:

comparing the field ranks of information segments in neighboring registers; and

wherein systolically moving information segments includes moving information segments between neighboring registers in response to the field rank comparisons.

8. The method of claim 7 further comprising:

inserting an information segment into a temporary register in a first stage;

comparing the field rank of the information segment in the temporary register to the field rank of an information segment in a first stage permanent register;

inserting the information segment having the lower rank into the temporary register of a second stage, higher in order than the first stage; and

wherein moving information segments between neighboring registers includes moving the information segment having the higher rank into the first stage permanent register.

9. The method of claim 8 further comprising:

extracting an information segment with the highest field rank from each stage.

10. The method of claim 9 wherein comparing the field ranks of information segments in neighboring registers includes comparing the field ranks of information segments in consecutive stages of the sequenced order of stages.

11. The method of 10 further comprising:

following the extraction of an information segment from a register in a first stage, forming a cooperative relationship between the first stage and a second stage, higher in sequence then the first stage.

12. The method of claim 11 further comprising;

comparing the field ranks of information segments in the cooperating first and second stages; and

following the comparison, moving the information segment with the highest ranking to the permanent register in the first stage.

13. The method of claim 12 wherein comparing the field ranks of information segments in the cooperating stages includes:

comparing the field rank of the information segment in the temporary register of the first stage to the information segment in the permanent register of the second stage;

simultaneously comparing the field rank of the information segment in the temporary register of the second stage to the information segment in the permanent register of the second stage; and

simultaneously comparing the field rank of the information segment in the temporary register of the first stage to the information segment in the temporary register of the second stage.

14. The method of claim 13 further comprising:

ignoring the result of a simultaneous comparison of information segments in neighboring registers if one of the registers is empty.

15. The method of claim 13 further comprising:

if the information segment in the first stage temporary register is not moved into the first stage permanent register, moving the information segment to the second stage temporary register.

16. The method of claim 13 further comprising:

if the information segment in the second stage permanent register is not moved into the first stage permanent register, maintaining the information in the second stage permanent register.

17. The method of claim 13 further comprising:

if the information in the second stage permanent register is moved into the first stage permanent register, forming a cooperative relationship between the second stage and a third stage, higher in sequence then the second stage.

18. The method of claim 7 wherein comparing of the field ranks of information segments in neighboring registers include selecting the first inserted information segment if the information segments have the same field rank.

19. The method of claim 9 wherein inserting an information segment includes inserting information segments at a maximum insertion rate.

20. The method of claim 19 wherein extracting an information segment includes extracting the information segments at a maximum insertion rate equal to twice the maximum extraction rate.

21. In an earliest deadline first (EDF) queue, a method for sorting information segments, the method comprising:

comparing the field rankings of information segments in neighboring registers;

in response to comparing, systolically moving information segments with lower field rankings to temporary registers higher in sequence; and

in response to comparing, systolically moving information segments with higher rankings to permanent registers lower in sequence.

22. The method of claim 21 further comprising:

extracting information segments at a maximum first rate; and

inserting information segments at a maximum second rate, twice the first rate.

23. The method of claim 22 further comprising:

pairing each temporary register to a permanent register having the same order in a sequence of registers, forming a sequence of stages;

in response to inserting an information segment into a temporary register in a first stage, comparing the field ranks of the information segments in the temporary and permanent registers of the first stage.

24. The method of 23 further comprising:

in response to extracting an information segment from a permanent register in a first stage, comparing the field ranks of an information segment in the first stage temporary to information segments in a second stage, higher in sequence than the first stage.

25. The method of claim 21 further comprising:

shifting information segments having the same field ranks.

26. In an earliest deadline first queue integrated circuit, a system for sorting information segments by field rank, the system comprising:

a sequence of stages for storing information segments having a field of sequential ranks;

wherein each stage has a port for accepting information segment insertions from a lower sequence stage, a port for supplying extracted information segments to a lower sequence stage, a port for accepting information segment extractions from a higher sequence stage, and a port for supplying information segment insertions into a higher sequence stage; and

wherein each stage accepts information segments inserted at a maximum insertion rate, and supplies information segments extracted in response to the field rank of the information segment, at a maximum extraction rate, where the maximum insertion rate is equal to twice the maximum extraction rate.

27. The system of claim 26 wherein each stage includes a temporary register having an input and an output, and a permanent register having an input and an output; and

wherein a lower sequence stage inserts information segments into the temporary register of a higher sequence stage.

28. The system of claim 27 wherein a permanent register in a lower sequence stage receives information segments extracted from a higher sequence stage.

29. The system of claim 28 wherein each stage further includes:

a first comparator having a first input connected to the temporary register output, a second input connected to the output of the permanent register, and an output to supply the results of a comparison of information segment field ranks;

a second comparator having a first input connected to the temporary register output, a second input connected to the output of a permanent register in a higher sequence stage, and an output to supply the results of a comparison of information segment field ranks; and

a third comparator having a first input connected to the temporary register output, a second input connected to the output of a temporary register in a higher sequence stage, and an output to supply the results of a comparison of information segment field ranks.

30. The system of claim 29 wherein each stage further includes:

a first multiplexor (MUX) having a first input connected to the output of the permanent register in the higher sequence stage, a second input connected to the temporary register in the higher sequence stage, a third input connected to the output of the temporary register in the same stage, a fourth input connected to the output of the permanent register in the same stage, an output connected to the input of the permanent register in the same stage, and a control input to accept MUX selection commands.

31. The system of claim 30 wherein each stage further includes:

a second MUX having a first input connected to the output of the permanent register in the same stage, a second input connected to the output of the temporary register in the same stage, an output connected to the input of the higher sequence stage temporary register input, and a control input to accept MUX selection commands.

32. In a earliest deadline first queue integrated circuit, a system for sorting information segments by field rank, the system comprising:

a sequence of stages for storing information segments having a field of sequential ranks;

wherein each stage includes a temporary register having an input and an output, a permanent register having an input and an output,

a port for accepting information segment insertions from a lower sequence stage, ports for supplying extracted information segments to a lower sequence stage, a port for accepting information segment extractions from a higher sequence stage, and a port for supplying information segment insertions into a higher sequence stage;

wherein each stage accepts information segments inserted into the temporary register from a lower sequence stage at a maximum insertion rate, and accepts information segments into the permanent register extracted from a higher sequence stage, in response to the field rank of the information segment, at a maximum extraction rate equal to one-half the maximum insertion rate;

wherein each stage includes a first comparator having a first input connected to the temporary register output, a second input connected to the output of the permanent register, and an output to supply the results of a comparison of information segment field ranks;

wherein each stage includes a second comparator having a first input connected to the temporary register output, a second input connected to the output of a permanent register in a higher sequence stage, and an output to supply the results of a comparison of information segment field ranks;

wherein each stage includes a third comparator having a first input connected to the temporary register output, a second input connected to the output of a temporary register in a higher sequence stage, and an output to supply the results of a comparison of information segment field ranks;

wherein each stage includes a first multiplexor (MUX) having a first input connected to the output of the permanent register in the higher sequence stage, a second input connected to the temporary register in the higher sequence stage, a third input connected to the output of the temporary register in the same stage, a fourth input connected to the output of the permanent register in the same stage, an output connected to the input of the permanent register in the same stage, and a control input to accept MUX selection commands;

wherein each stage includes a second MUX having a first input connected to the output of the permanent register in the same stage, a second input connected to the output of the temporary register in the same stage, an output connected to the input of the higher sequence stage temporary register input, and a control input to accept MUX selection commands; and

wherein each stage includes a controller having a first input connected to the output of the first comparator, a second input connected to the output of the second comparator, a third input connected to the output of the third comparator, a fourth input to connected to the output of a second comparator in a lower sequence stage, a fifth input connected to the output of a third comparator in a lower sequence stage, a sixth input connected to the output of a first comparator in a higher sequence stage, a seventh input to accept insertion and extraction commands from a controller in a lower sequence stage, a first output connected to the control input of the first MUX, a second output connected to the control input of the second MUX, and a third output connected to the seventh input of a controller in a higher sequence stage.

33. The system of claim 32 wherein the controllers in the sequence of stages interact to systolically move information segments with lower field ranks from stages lower in a sequence, to stages higher in sequence.

34. The system of claim 33 wherein the controllers in the sequence of stages cooperate as a team to systolically move information segments with higher field ranks, from higher sequence stages, to lower sequence stages.

35. The system of claim 33 wherein each controller has an eighth input connected to the seventh input of a controller in a lower sequence stage to further cooperation between the controllers.

36. The system of claim 35 wherein an information segment is inserted into a temporary register in a first stage;

wherein the first comparator compares the ranks of the information segment inserted into the temporary register and the information segment in the permanent register, and supplies the results of the comparison to the controller;

wherein the controller directs the first MUX to supply the information segment with the higher rank to the permanent register; and

wherein the controller directs the second MUX to supply the information segment with the lower rank to a temporary register of a second stage, higher in sequence than the first stage.

37. The system of claim 36 wherein an information segment is extracted from the first stage permanent register;

wherein the first stage second comparator compares the rank of the information segment in the first stage temporary register to an information segment in the second stage permanent register;

wherein the first stage third comparator compares the rank of the information segment in the first stage temporary register to the information segment in a second stage temporary register; and

wherein the second stage first comparator compares the rank of the information segment in the second stage temporary register to the information segment in the second stage permanent register.

38. The system of claim 37 wherein the controller disregards the output of a comparator, if that comparator is comparing a register having no information segment.

39. The system of claim 37 wherein the first stage controller sends a message to the second stage controller communicating the extraction operation;

wherein the first stage controller directs the first stage first MUX to deliver the highest ranking information segment to the first stage permanent register; and

wherein, if the first stage temporary register information segment is not the highest ranked, the first stage controller directs the

first stage second MUX to insert that information segment into the second stage temporary register.

40. The system of claim 37 wherein, if the second stage permanent register information segment is not the highest ranked, the first stage controller maintains that information segment in the second stage permanent register.

41. The system of claim 37 wherein, if the second stage permanent register information segment is extracted and moved to the first stage permanent register, the second stage second comparator compares the rank of the information segment in the second stage temporary register to an information segment in a third stage permanent register, where the third stage is higher in sequence than the second stage;

wherein the second stage third comparator compares the rank of the information segment in the second stage temporary register to the information segment in a third stage temporary register; and

wherein the third stage first comparator compares the rank of the information segment in the third stage temporary register to the information segment in the third stage permanent register.

42. The system of claim 37 wherein the first stage controller sends a message to the second stage controller communicating the insertion operation;

wherein the first stage controller directs the first stage second MUX to deliver an information segment for insertion into the second stage temporary register.

43. The system of claim 32 wherein the temporary register of a first stage receives a shift command from a stage lower in the sequence of stages, and an information segment having the same rank as the information segment in the first stage permanent register; and

wherein the information segment in the first stage permanent register is shifted to a temporary register in a second stage, higher in the sequence of stages than the first stage.

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